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Design and Implementation of Submicron Level 10T Full Adder in ALU Using Cell Based and SOC Technology

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ABSTRACT
As technology scales into the nanometer regime leakage current, active power, delay and area are becoming important metric for the analysis and design of complex circuits. The main concern in mobile and battery based systems are leakage current and power dissipation. A transistor resizing approach for 10 transistor single bit full adder cells is used to determine optimal sleep transistor size which reduces power dissipation and leakage current. A submicron level 10-transistor single bit full adder cell is considered to achieve low leakage current, reduced power dissipation and high speed. In this paper initially 10T full adder cell is designed with submicron technique and later this is employed to design an ALU adder unit. The modified ALU is simulated and synthesized successfully on cadence 180nm technology.
Keywords - Low leakage, cmos, 10T full adder, sleep transistors, carry lookahead adder, SoC(system on chip).

I.   INTRODUCTION

Adders are important and heart of computational circuits. Many of complex arithmetic circuits are based on addition and it is often one of the speed limiting elements [1]. Hence, optimization of the adder in speed and power consumption must be pursued. These adder cells aimed to reduce power consumption and increase speed.

In digital electronic systems, Arithmetic logic unit(ALU) is a digital circuit that performs arithmetic and logical operations. John von neumann who proposed the ALU in 1945 when he was working on electronic discrete variable automatic computer. ALU is a fundamental building block of central processing unit of a computer, and even the simplest microprocessors contain one or more circuits for timers. It is one of the many components within a computer processor and performs mathematical, logical, and decision operations in a computer and is the final processing performed by the processor. After the information has been processed by an ALU and sent to the computer memory . In some computer processors
ALU is divided into an arithmetic and logic unit. The arithmetic unit performs the arithmetic operations and the logic unit performs the logical operations.ALU(Arithmetic logic unit) is an integrated circuit in CPU(central processing unit) that performs arithmetic and logic operations. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include AND, OR and NOT operations. For the division operation, it may result fraction, or floating point number. Instead,

division operations are usually handled by the floating point unit, which also performs other non-integer calculations. Some of the processors contain single ALU while others include many arithmetic logic units that work together to perform calculations . Regardless of the way an ALU is designed its primary job is to handle integer operations, and therefore, a computer's integer performance is tied directly to the processing speed of ALU.

In this paper a low leakage 10T one-bit full adder cell is employed in CLA to implement an ALU. A transistor resizing approach for 1bit full adder cells is introduced to determine the optimal sleep transistor size which reduces the leakage current thereby power dissipation is reduced.

II.   SUBMICRON AND OPTIMIZED SLEEP TRANSISTOR

Micron is the measurement of length. The length between the source and drain (Lmin is between 10nm to 45nm). Submicron technology allows millions of transistors on a die running at GHz frequencies. Submicron condition is subthreshold condition.
Categories of CMOS technology:
1.)Submicron technology –Lmin>= 0.35 microns
2.)Deep Submicron technology (DSM) – 0.1 microns<= Lmin<=0.35 microns
3.)Ultra-Deep Submicron technology (UDSM) – Lmin<= 0.1 microns

sleep transistor is a PMOS or NMOS high Vth transistor and is used as a switch to shut off power

supplies to parts of the design in standby mode and although the concept of the sleep transistor is straight forward, the optimal sleep transistor design and implementation are a challenge due to various effects, introduced by the sleep transistor and its implementations on design performance, area, routability, overall power dissipation, and signal/power integrity.

Sleep transistors are to reduce power and heat dissipation, but not to reduce leakage currents. Quality of sleep transistor design is often measured in terms of three metrics: which are switch efficiency, area efficiency and IR drop. The sleep transistor is optimized in gate length, width, finger size and body bias to achieve high switch and area efficiencies, and low leakage current and IR drop. Sleep mode refers to a low power mode for electronic devices such as computers, televisions, and remote controlled devices.

III. 10T FULL ADDER WITH REVERSE BIAS

10-transistor one bit full adder circuit with self-reverse biasing technique [1] is shown in Fig.1. The circuit of 10T adder has three inputs and two outputs (A, B, C, sum, Cout). The whole circuit works with single supply Vdd. The number of direct connections from Vdd and ground is reduced in this design to minimize the power consumption due to short circuit current. In this circuit body of 5 nmos is connected to external voltage supply to act as sleep transistor. The nmos transistor goes to sleep mode due to increase in threshold voltage. In active mode of operation the high Vth transistors are turned off and the logic gates consisting of low Vth transistors can operate with low switching power dissipation and smaller propagation delay. In standby mode the high Vth transistors are turned off thereby cutting off the internal low Vth circuitry.

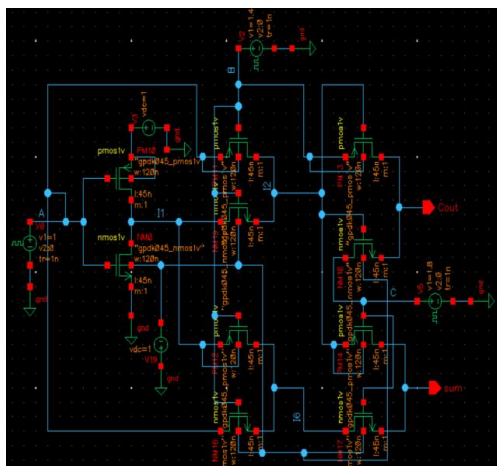Sum=A.B̄ .C̄ + Ā .B̄ .C + Ā . B̄ .C̄ + A. B.C

Cout=A.B + B.C+ C.A

Fig. 1. 10T Full Adder cell with self-reverse bias[1]

Transistor creates negative voltage at the body by proper design rules and increasing Vth by body bias which goes to cutoff state and as there is no conduction in reverse bias leakage current will be reduced.

$$V_{th} = V_{t0} + \gamma \left(\sqrt{|V_{sb} + 2\emptyset_f|} - \sqrt{|2\emptyset_f|} \right)$$

Where V_{th} is threshold voltage when body bias is present, V_{sb} is source to body bias, $2\emptyset_f$ is surface potential, and V_{t0} is threshold voltage of zero substrate bias, $\gamma = \left(\frac{t_{ox}}{e_{ox}}\right)\sqrt{2qe_{si}N_A}$ is body effect parameter, t_{ox} is oxide thickness, e_{ox} is oxide permittivity, e_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of electron.

The body effect in CMOS transistors changes with the change in threshold voltage, a smaller width of the depletion layer decreases Vth. In reverse bias CMOS transistor increases Vth, while on forward biasing of the CMOS transistor Vth decreases. And in CMOS threshold voltage increases with the increased doping of the channel but decreases with applied bias. Therefore, the current in the subthreshold region can be decreased by reverse bias.

IV. ALU DESIGN

In the design of ALU the 10T one bit full adder circuit with self-reverse bias is used in CLA to implement an ALU with FIFO as memory and the whole process is done in cadence. Implemented ALU in SOC technology using LEF file generation in cadence 180nm technology. Simulated 8-bit carry lookahead and 8-bit FIFO program for ALU is shown in fig.2. Simulations are performed in cadence IUS (incisive unified simulator). For low power RTL synthesis are performed in cadence RTL and later SoC is done in cadence encounter.
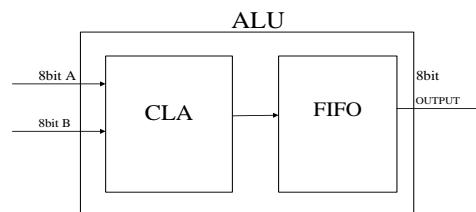

Fig. 2. Block diagram of ALU with CLA and FIFO in cadence IUS.

V. RESULTS

Simulations are performed in cadence 180nm technology.
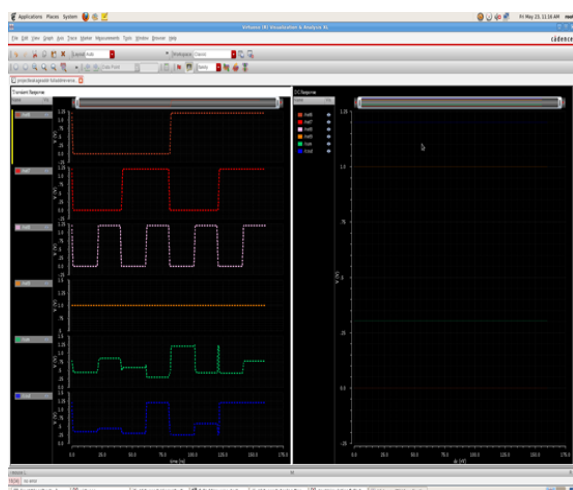Simulation of 10T full adder with self reverse bias in cadence virtuoso:

Fig. 3. Waveform of 10T full adder with reverse bias simulation

Fig.3 shows the waveform of 10T full adder the first 3 waveforms are inputs a, b, c and last 2 waveforms are outputs sum and Cout. X-axis is time period in nanoseconds and Y-axis is voltage in volts. This is the waveform of reduced parasites after post layout simulation.
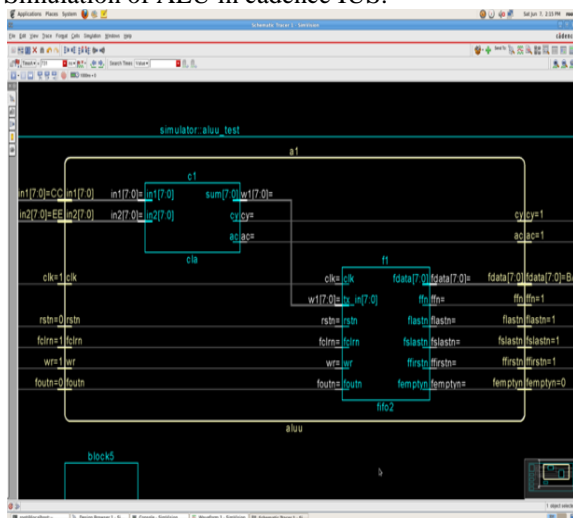
Simulation of ALU in cadence IUS:

Fig. 4. Block diagram of ALU

Fig.4 is the block diagram of ALU in which the 8bit CLA and FIFO are integrated in the ALU block in which the CLA output is connected to FIFO input where the SUM generated by CLA is stored in FIFO and appears at the output when the clock is active.
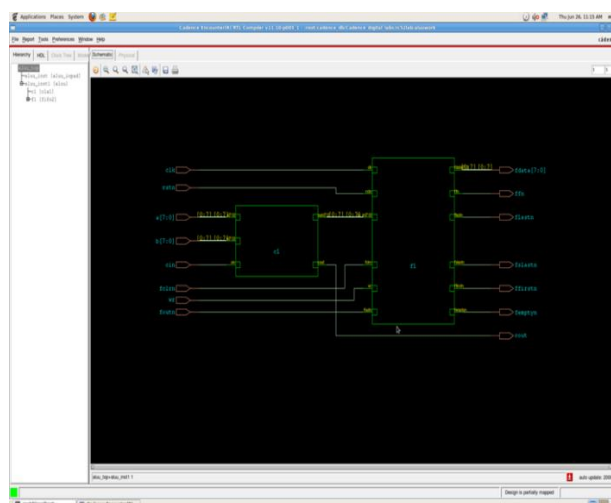
RTL synthesis of ALU:

Fig. 5. Block diagram of ALU in cadence encounter

Fig.5 above shows the block diagram of ALU after RTL synthesis in cadence encounter. Register transfer level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Here creating LEF file for 10T full adder reverse bias and attaching the LEF file for ALU which gives reduced leakage power and without attaching the LEF file for ALU shows the result.

Top module of ALU with ALU and IOPAD programming in RTL Encounter:
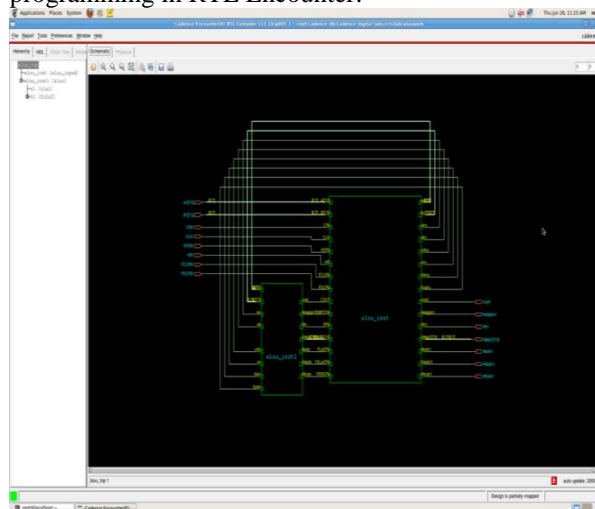

Fig. 6. ALU in RTL encounter

Fig.6 shows the block diagram of ALU top module in which ALU with RTL synthesis and ALU with iopad programming is done in order to secure ALU from damage.
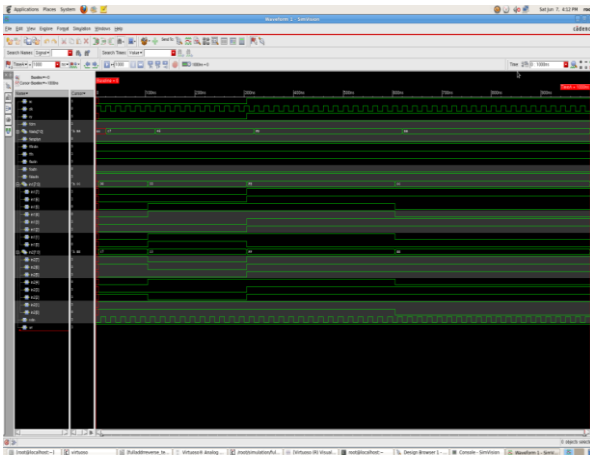
Waveforms of ALU :

Fig. 7. Output waveform of ALU

Fig.7 shows waveform of ALU with 8bit inputs A, B with 8bit output as SUM which consists of CLA and FIFO.

Simulated Power Analysis of ALU:

Simulations	Leakage power(uW)
ALU	17.526
ALU with submicron level 10T full adder with reverse bias	2.745

These are the simulation results of ALU designed with CLA and FIFO with and without attached 10T full adder reverse bias in ALU with generated LEF file. By adding 10T full adder reverse bias LEF file the leakage power is reduced to 17.526uW to 2.745uW.
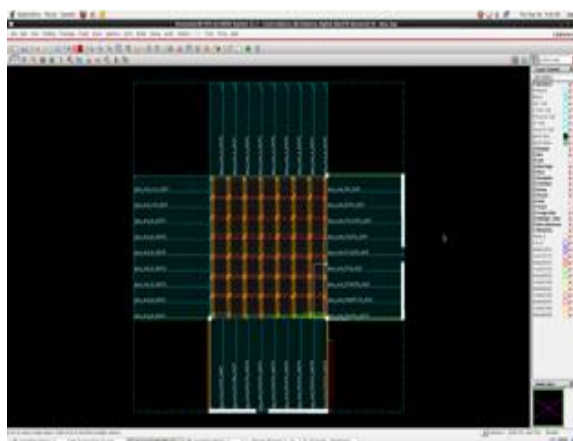
SoC results of ALU:

Fig. 8. Chip design layout of ALU in SoC

The above fig.8 shows layout of chip design of ALU employed with submicron level 10-transistor full adder is implemented in the cadence SoC Encounter. After getting the results in cadence virtuoso, IUS and RTL compiler the chip design is done in SoC encounter by creating LEF file for 10T full adder with reverse bias circuit in virtuoso and netlist for designed ALU in RTL compiler. The ALU chip design for SOC is achieved by combining LEF file and netlist in cadence SOC encounter tool.

VI. CONCLUSION

Submicron level low leakage single bit full adder cell is proposed for mobile and battery based systems and the full adder employed in ALU is proposed for processors. By using optimal sleep transistors and transistor resizing technique, leakage current is reduced, thereby power dissipation is reduced when compared to conventional cmos adders. Using this technique active power reduction is achieved in the ALU with low leakage. The design of ALU is realized in cadence 180nm cmos technology, in short design of ALU can be a better alternative.

VII. FUTURE SCOPE

ALU employed with submicron level 10T full adder can be implemented in advanced RISC processor and high end processors to reduce power dissipation. Deep submicron full adder can be used in the encryption algorithm for security purpose. 10 transistor full adder can be used in image processing technology.

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